COMPARATIVE ANALYSIS OF LEAKAGE REDUCTION OF BENCHMARK CIRCUITS FOR DEFENSE APPLICATIONS

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ABSTRACT: Design complexity is increasing day by day in modern electronic systems. Due to reconfigurable architecture, low non recurring engineering (NRE) and ease of design Field Programmable Gate Arrays (FPGA) become a better solution for managing increasing design complexity. This paper provides a detailed comparative analysis of leakage of various benchmark circuits for defense applications. We have implemented a benchmark circuits (C6288) 16 * 16 multiplier and C880 (8-bit ALU) in Defense Grade Spartan-6Q Lower Power FPGA. Various enhanced power gating schemes has been imposed on LUT to analysis leakage. As compared to basic design, proposed design saves 15% of leakage power.

KEYWORDS: Field Programmable Gate Arrays (FPGA), Look Up Table, Leakage Reduction.

INTRODUCTION

The biggest challenge for FPGAs implemented in nanometer CMOS technologies is the increasing power dissipation and in particular, leakage power. Also, as we go down to technology ground bounce noise also become important metric of comparable importance to active power, delay and area for the analysis and design of battery operated devices.

Traditionally, leakage power reduction in FPGAs has been overshadowed by an interest in reducing the dynamic power dissipation and improving the overall performance. Recently, several research projects have been conducted to mitigate the leakage power reduction in FPGAs. The most popular of these techniques employs dual Vdd, transistor sizing, dual Vth, body biasing, multihreshold CMOS (MTCMOS), and input vector forcing.

Due to the scaling trends and to support reconfigurability, FPGA uses more transistors which increase the leakage power consumption as compared to ASIC. As we know that leakage power is proportional to the total number of transistor count and so the leakage optimization of FPGA becomes one of the major design challenges for future FPGA technologies. In this paper, we provide a performance analysis of c6288 and C880 benchmark circuit. We have implemented benchmark circuits on Defense Grade Spartan-6Q Lower Power FPGA.

Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground) [1], [2], [3]. This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance [4], [5], [6] and further peak of ground bounce noise is possible with proposed novel technique. The biggest challenge for FPGAs implemented in nanometer CMOS technologies is the increasing power dissipation and, in particular, leakage power and ground bounce noise. Leakage power dissipation exponentially increases with the CMOS process scaling and is expected to dominate the total chip power dissipation in deep submicron CMOS process. To mitigate the leakage problem, power gating is widely implemented to suppress the leakage power in standby mode. Sleep transistors (ST), which are used to gate the power, deteriorate the noise characteristic of the circuits because their drain to source voltage drop changes the virtual rails of the circuit [7], [8], [9]. Furthermore, during the mode transitions: especially from sleep mode to active mode, the power gating schemes cause large power and ground bounce that greatly affects the reliability of the circuits nearby in a mixed signal design. It is therefore essential to consider using techniques such as power gating to address the problem of ground bounce in low-voltage CMOS circuits [10] – [14].

This paper focuses on reducing leakage power of low Power FPGA devices for defense application using enhanced power gating schemes so that these benchmark circuits can be used for defense application devices. The rest of the paper is organizes as follows: In section II we discuss the related contribution of leakage reduction in the field of FPGA. Section III, provides the simulation results of leakage reduction of LUT of various benchmark circuit for FPGA devices for defense applications and finally the paper is concluded in section IV.

RELATED WORK

Spartan®-6Q defense-grade FPGAs support the high security requirements of Information Assurance and Anti-tamper in Aerospace and Defense (A&D) applications. As the third generation of secure defense-grade reprogrammable devices, the family is an ideal platform for MILCOM and other applications where security, low-power and low-costs are paramount.

The Spartan-6Q family is the third generation of secure product offered for high-level cryptography and tamper proofing approved by government agencies. Built on a mature 45 nm low-power copper process technology that delivers the optimal balance of cost, power, and performance, the Spartan-6Q family offers a more efficient, dual-register 6-input look-up table (LUT) logic and a rich selection of built-in system-level blocks. These include 18 Kb (2 x 9 Kb) block RAMs, second generation DSP48A1 slices, SDRAM memory controllers, enhanced mixed-mode clock management blocks, SelectIO™ technology, power-optimized high-speed serial transceiver blocks, PCI Express® compatible Endpoint blocks, advanced system-level power management modes, auto-detect configuration options, and enhanced IP security with AES and Device DNA protection. These features provide a low-cost programmable alternative to custom ASIC products with unprecedented ease of use. Spartan-6Q FPGAs offer the best possible solution for defense related applications where SWaP-C reduction is paramount with absolute security and ruggedized environment operation [15].

A variety of power reduction techniques have been proposed in literature. The basic idea of the leakage power is described in [16]. The simulation methodology accounts for design. Here a detailed leakage power of a low cost 90nm FPGA is described by device level simulation. The paper describes about the percentage of resource utilization in FPGA and the total power consumption of a particular configurable logic block (CLB). Many of the recent works also described FPGA power consumption [17] - [20] and have shown that power consumed by the current FPGA device is increasing, with such devices consuming watts of power.

V.K Sirigir et al [21] present a novel complementary Nano-Electro-Mechanical (CNEM) switch that operates with virtually zero leakage current and has 1 to 2 volts operating voltage. He analyzed the impact of the CNEM substitution on power and delay using VPR and the MCNC benchmark circuits. The experimental results shows an average 98%, 85%, 71% and 99.9% reduction in critical path delay, routing energy, total energy, leakage power when comparisons are made between FPGA design using pure CMOS technology.

R. Jaramillo et al [22] proposes and evaluates ten routing designs based on the dual threshold technique to reduce leakage power. He analyzes the percentage constitution of low-Vth and high Vth transistors as a function of the leakage reduction and delay increment tradeoff. By routing a suite of MCNC benchmark circuits an average saving of 28.83% in total inter connect leakage has been done.

H. Keheng et al [23] focuses on reducing the leakage power in routing resources. They observed that the leakage power in off-path transistors takes up most of the active leakage power in multiplexers that control routing, and strongly depends on hamming distance between the state of the on-path input and the states of the off-path inputs. The proposed off path leakage power aware routing algorithm reduce active leakage power in routing resources by 16.79%.

A. Chakorabarty et al [24], presents the first placement algorithm to specifically target leakage problem. Power aware structures ASIC placement tool minimizes the clock and leakage power by maximizing the fraction of the structures ASIC that can be powered down or disconnected from clock tree. On a set of large benchmark designs, PASAP reduces a clock and leakage by 32% and 17% respectively.

PERFORMANCE ANLAYSIS AND SIMULATION RESULTS

The performance analysis of LUT of benchmark circuit C6288 (16*16 multiplier) and C880 (8-bit ALU) on Defense-Grade Spartan-6Q Lower power FPGA devices. Table I shows the details of resource utilization summary of benchmark circuits on above mentioned FPGAs. The performance analysis for leakage current of LUT on FPGA device has been done using Xilinx ISE 14.2 is shown in Table II.

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look-up table (LUT) logic and a rich selection of built-in system-level blocks. These include 18 Kb (2 x 9 Kb) block RAMs, second generation DSP48A1 slices, SDRAM memory controllers, enhanced mixed-mode clock management blocks, Select IO™ technology, power-optimized high-speed serial transceiver blocks, PCI Express® compatible Endpoint blocks, advanced system-level power management modes, auto-detect configuration options, and enhanced IP security with AES and Device DNA protection. These features provide a low-cost programmable alternative to custom ASIC products with unprecedented ease of use. Spartan-6Q FPGAs offer the best possible solution for defense related applications where SWaP-C reduction is paramount with absolute security and ruggedized environment operation [15].

The resource utilization summary of benchmark circuits is given in Table 1. All the results has been analyzed using XILINX ISE 14.2. Table III clearly depicts the simulation results of leakage power analysis of benchmark circuit using defense device. From table it is clear that leakage power is reduced in C880 benchmark circuit as on compared to C6288. The leakage power is reduced by 15%. Hence from the simulation results it is clear that C880 benchmark circuits is most suitable for defense applications.

Table 1: Resource Utilization Summary of LUT of C6288 and C880 Benchmark Circuit for Defense Device SPARTAN 6Q

Benchmark Circuits	No. of Slices Used	Used LUTs	No. of IOs	No. of Bonded IOBs
C6288	422 out of 704	740 out of 1408	64	64 out of 108
C880				

Table 2: Comparison of Leakage Power of LUT of C6288 and C880 Benchmark Circuit for Defense Applications

Benchmark Circuit	Leakage Current
C6288	339.36nW
C880	215.32nW

CONCLUSION

This paper provides a detailed analysis of benchmark circuit c6288 (16 * 16 Multiplier) and C880 (8 bit ALU) for defense applications. The paper reveals that by using proposed benchmark circuits the leakage power is reduced by 15% as on compared to prevalent benchmark circuits. Hence, these benchmark circuits are suitable or can be used for defense applications.

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